judging whether or not to rewrite said third pixel data corresponding to said second depth data stored in said storage circuit with said second pixel data on the basis of the result of the comparison; and

stopping the operation of at least one of said pixel processing circuits when judging that the corresponding pixel is not positioned within said graphic unit to be processed or when judging not to rewrite.

IN THE DRAWINGS:

A separate Letter to the Official Draftsperson is being filed herewith to amend the reference numerals and text in Figs. 1, 4, 5, 7, 8 and 11 of the drawings for this application. Entry of these amendments is respectfully requested.

REMARKS

This is in full and timely response to the Office Action dated July 31, 2001. Reconsideration and reexamination are respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1 to 7, 9 to 12, 14, 16, 18, 21 to 23, 25, 27, 28, 31, 32, 35, 37, 39 and 40 have been amended. Claims 1 to 40 remain pending for the Examiner's reconsideration.

Attached hereto is a marked-up version of the changes made to the specification

and claims by the current amendment. The attachment is captioned "Version with Markings to Show Changes Made."

As requested by the Examiner on page 2 of the Office Action, the title of the invention has been amended to be more descriptive and indicative of the invention to which the claims are directed. The amended title reads as follows: "IMAGE PROCESSING APPARATUS AND METHOD OF PROCESSING IMAGES THAT STOPS OPERATION OF PIXEL PROCESSING CIRCUITS WHEN PIXEL DATA TO BE PROCESSED IS NOT NEEDED." It is respectfully submitted that the title, as amended, is sufficiently descriptive of the Applicant's invention.

The specification has been carefully reviewed and amended to correct minor informalities, including grammar and syntax. For example, "an" has been changed to --a-- where appropriate; the phrase "Fig. 6" on page 29, line 25, has been changed to --Fig. 12-- which is the drawing that shows the described block 31; reference numeral 11 has been added to page 44, line 8, for the triangle DDA circuit shown in Fig. 7; the phrase "as shown in Fig. 9" has been added to page 53, line 9, to make proper reference to the circuit shown in Fig. 9 of the drawings; and the phrase "was given" was added page 55, line 5, to correct the sentence structure. Moreover, the reference numerals/characters have been corrected at several places in the specification to correspond more accurately with the drawings and the other parts of the specification. The specific reasons for these changes are believed to be self-explanatory from a review of the original specification and the marked-up version attached hereto showing each of the changes.

Claims 16 and 35 were objected to for having a typographical error in the last step of these claims. To overcome this objection, claims 16 and 35 have been amended to change the phrase "blending will not be not performed" in the last step into --blending will not be performed--. Reconsideration and withdrawal of this objection are respectfully requested.

The claims were also reviewed and amended to further clarify the claimed invention and correct minor informalities in the claim language. For example, several of the claims (e.g., claims 1, 2, 5, 7, 21, 22, 25, 32 and 40) were amended to change the phrase "pixel processing circuit" into --pixel processing circuits-- to be consistent with the claimed "plurality of pixel processing circuits" recited in the independent base claims. Claim 3 was amended to change the phrase "plurality series connected processing circuits formed as" into --plurality of processing circuits connected in series to form-- to clarify this claimed feature. Claims 6, 16, 21, 27, 35 and 40 were amended to change the phrase "the same said graphic unit" into --each graphic unit-- to correct a potential lack of antecedent basis. Claim 11 was amended to change "image processing circuits" into --pixel processing circuits-- to be consistent with the other claim language. Claim 12 was amended to change the phrase "said pixel processing circuit" into --each respective pixel processing circuit-- to correct a potential lack of antecedent basis. Claim 31 was amended to change the phrase "the corresponding pixel processing circuits" into --at least one of said pixel processing circuits-- to correct a potential lack of antecedent basis. Claim 32 was amended to delete the extraneous "operating" step. Claim 39 was amended to depend upon claim 38 instead of claim 37. Other minor amendments were made throughout the claims to

place them in better condition for further examination and allowance.

In the separate Letter to the Official Draftsperson being filed herewith, several minor amendments were proposed to the reference numerals and text in Figs. 1, 4, 5, 7, 8 and 11 of the drawings. These amendments are supported by the corresponding text of the specification, and further explanation of each change is not believed to be necessary.

Claims 1 to 3, 5 to 8, 10, 22 to 24 and 26 to 29 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dawson et al. (U.S. Patent No. 5,179,638) in view of Kiyoto (JP Publication No. 09130570). The Examiner contends that Dawson et al. teaches an image processing apparatus having all of the features of the Applicant's claimed invention, except for a means for stopping the operation of the pixel processing circuits for pixels that do not lie within the graphic units. The Examiner relies upon Kiyoto for a teaching of this feature. This rejection is respectfully traversed for the following reasons.

Dawson et al. discloses an image processing apparatus for providing a texture mapped perspective view for digital map systems. Dawson et al.'s system includes means for storing elevation data and texture data, means for scanning a projected view volume from the elevation data storing means, means for processing the projected view volume, means for generating a plurality of planar polygons, and means for rendering images.

The image processing system of Dawson et al. uses a rendering engine 34 that receives an input of coordinates for planar polygons from a tiling engine 40, and then generates image data across each polygon by interpolating color, depth, elevation, and transparency from

pixels on the edges of the polygon (see column 8, lines 26 to 65). This is an image processing technique referred to as "polygon rendering," which is described in the Background section of the Applicant's specification (see page 1, line 22, through page 2, line 8).

In conventional polygon rendering, such as that performed by the engine 34 of Dawson et al., processing is performed in parallel (simultaneously) for all pixels in a predetermined block. Since some of the pixels in a predetermined block fall outside the polygon being rendered and are not needed, the operations performed on these pixels become invalid. In imaging devices such as the device described by Dawson et al., processing is performed on all of the plurality of pixels located in a predetermined block regardless of whether they are inside the polygon or not. Thus, a large number of invalid operations are performed and power consumption is increased.

Kiyoto fails to remedy the deficiencies in the image processing system of Dawson et al. Kiyoto discloses an image forming device (e.g., a color copying machine) which includes a scanner, a printer, and an image processing means. The device includes an image processing means which receives and processes image data based on picture image clock signals for each processing block that receives image data from an external device, such as a scanner. A supply/inhibit signal is used to inhibit application of the image clock signal to processing blocks that do not receive image data. By stopping application of the image clock signal to processing blocks which are not in use, power consumption of the image forming device is reduced.

In the image processing device of Kiyoto, the image clock signal is inhibited for

an entire processing block, and not just for selected pixels or pixel processing circuits within a processing block. This is a significant distinction between the Applicant's claimed invention and the teachings of Kiyoto. If the teachings of Kiyoto could somehow be applied to image the polygon 30 shown in Fig. 12 of the Applicant's drawings, the rendering would be performed unconditionally on all of the pixels in the blocks 31, 32, and 33 because at least part of the pixels of each block 31, 32, 33 are within the polygon 30. As a result, a large number of invalid operations would occur and power consumption would be substantially higher than required by the Applicant's invention.

Moreover, Kiyoto does not teach an image processing device for use with "polygon rendering." The image processing device of Kiyoto was apparently developed for color copying machines and the like, and not for three-dimensional computer graphics and the like which use polygon rendering techniques. There is no teaching or suggestion in Kiyoto of stopping an image clock signal to selected pixel processing circuits of a plurality of pixels to be processed simultaneously (i.e., within a processing block), nor of stopping an image clock signal to a selected pixel processing circuit based on a judgment that the corresponding pixel is positioned outside a graphic unit to be processed.

It would not have been obvious to modify the image processing device of Dawson et al. based on the teachings of Kiyoto to arrive at the Applicant's claimed invention. As explained above, there is no teaching in either of these applied references of an image processing device having a means for stopping operation of selected pixel processing circuits within a group

of pixels to be processed simultaneously based on a judgment that the corresponding pixel is positioned outside the graphic unit to be processed. While Dawson et al. teaches image processing using polygon rendering methods, it is only representative of the related art image processing techniques described by the Applicant on pages 1 to 4 of the specification. On the other hand, Kiyoto does not even relate to imaging devices that use polygon rendering methods, and therefore has little relevance to the Applicant's claimed invention.

Accordingly, reconsideration and withdrawal of the rejection of claims 1 to 3, 5 to 8, 10, 22 to 24, and 26 to 29 based on Dawson et al. and Kiyoto are respectfully requested.

Claims 4, 9, 25 and 30 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dawson et al. in view of Kiyoto, as applied to claim 27, and further in view of Duluk, Jr. (U.S. Patent No. 5,977,987). The Examiner relies upon Duluk, Jr. for a teaching of connecting a flag storage portion to a shift register in series to control pipeline processing. This rejection is respectfully traversed for the following reasons.

Claims 4, 9, 25 and 30 are dependent, directly or indirectly, on independent claims 1, 6, 22 and 27, respectively. Therefore, it is respectfully submitted that these claims are allowable over the cited references for at least the same reasons explained above concerning independent claims 1, 6, 22 and 27. It is further noted that the image processing system disclosed by Duluk, Jr. does not have a means for stopping operation of selected pixel processing circuits within a group of pixels to be processed simultaneously based on a judgment that the corresponding pixel is positioned outside the graphic unit to be processed. Thus, Duluk, Jr. fails

to remedy the deficiencies in the combined teachings of Dawson et al. and Kiyoto, as explained above.

Accordingly, reconsideration and withdrawal of the rejection of claims 4, 9, 25 and 30 based on Dawson, Kiyoto and Duluk, Jr. are respectfully requested.

Claims 11 to 13, 15 to 19, 21, 31 to 33, 35 to 38 and 40 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dawson et al. in view of Huxley (U.S. Patent No. 5,742,796) and Kiyoto. This rejection is respectfully traversed for the following reasons.

Independent claims 11 and 31 recite an image processing apparatus and method, respectively, which use a plurality of pixel processing circuits to simultaneously blend a plurality of first and second pixel data based on a blending ratio data set for each pixel; judge based on the blending ratio data whether to perform the blending by pixel processing circuits; and stop the operation of the corresponding pixel circuits when judging that they will not perform the blending. The cited references fail to teach these features of the Applicant's invention.

The image processing method disclosed by Dawson et al. is described above. As noted by the Examiner, Dawson et al. fails to teach the use of blending ratio data in pixel processing. While Huxley does teach the use of blending ratio data in pixel processing, Huxley does not teach or suggest a control circuit or process step that judges whether or not the pixel processing circuits will perform blending, and then stops the operation of respective pixel processing circuits in which blending will not be performed.

Huxley discloses an image processing method having an alpha blend unit which

blends the source color and the destination color according to an alpha blend equation to produce an output color (see column 61, lines 5 to 67). As noted by the Examiner, Huxley also mentions the use of a NoAlphaBuffer bit in the AlphaBlendMode message when no alpha buffer is present. However, Huxley does not teach a system or method in which a determination is made whether alpha blending will be performed by the pixel processing circuits, nor in which the pixel processing circuits that will not perform alpha blending are stopped based on such a determination. Instead, it appears that the pixel processing circuits in Huxley continue processing the data unless the alpha blend mode is completely disabled (column 61, lines 65 to 67).

Claims 12 and 32, which depend upon claims 11 and 31, respectively, are allowable over the cited references for the following additional reasons. Claims 12 and 32 recite an image processing apparatus and method, respectively, in which the supply of clock signal to a pixel processing circuit is stopped when it is judged that the circuit will not perform blending of the first and second pixel data.

Huxley does not teach or suggest a system in which a clock signal is stopped to stop the operation of a pixel processing circuit after determining that it will not perform alpha blending. In fact, Huxley appears to teach away from such a system in column 7, lines 11 to 15, by stating that messages should continue to be passed on to other units even after determining a pixel is not going to be updated.

Similarly, the combined teachings of Dawson et al. and Kiyoto lack any teaching

or suggestion of an image processing system in which clock signals for individual pixel processing circuits in a block of such circuits to be processed simultaneously are selectively stopped based on a judgment that blending or other processing is not required of such pixel processing circuit.

Independent claims 16 and 35 recite an image processing apparatus and method, respectively, in which an image is expressed as a composite of graphic units of predetermined shape, a plurality of pixel processing circuits are used to blend a plurality of first and second pixel data based on a blending ratio data set, a control circuit judges whether or not a pixel is positioned within a graphic unit to be processed for each of the pixels being simultaneously processed, and the control circuit stops the operation of pixel processing circuits for pixels outside of the graphic units or those in which it is determined that blending will not be performed.

Claims 16 and 35 are allowable over the cited references for generally the same reasons explained above regarding these cited references. Specifically, none of the cited references teach stopping the operation of pixel processing circuits that are judged to lie outside of the graphic unit to be processed, as in the Applicant's invention. As explained above, Kiyoto fails to teach this feature of the claimed invention because in Kiyoto, the image clock signal is stopped for an entire processing block, and not for selected processing circuits within the processing block. Moreover, the teachings of Kiyoto are directed to color copiers, scanners and the like and have little relevance to the three-dimensional image processing technology of the

Dawson et al. and Huxley references.

Independent claims 17 and 36 recite an image processing apparatus and method, respectively, in which a plurality of pixel processing circuits are used to produce a plurality of second pixel data from a plurality of first pixel data, first depth data of the first pixel data is compared with second depth data of a plurality of third data stored in a storage circuit, and a control circuit judges whether or not to rewrite the third pixel data by the second pixel data and stops the operation of the corresponding pixel circuits when judging that they will not perform the rewrite.

The image processing systems disclosed by each of the cited references is described above. As noted by the Examiner, Dawson et al. fails to teach depth comparison between pixel data. While Huxley does teach the use of depth comparison between pixel data, Huxley does not teach or suggest the claimed circuit control recited in claims 17 and 36. Specifically, Huxley does not disclose a process step that judges whether or not to rewrite the depth data stored in the storage circuit by the first depth data, and then stops the operation of respective pixel processing circuits in which the depth data will not be rewritten. As explained above, Huxley appears to teach away from such a system in column 7, lines 11 to 15, by stating that messages should continue to be passed on to other units even after determining a pixel is not going to be updated.

Claims 18 and 37, which depend upon claims 17 and 36, respectively, are allowable over the cited references for the following additional reasons. Claims 18 and 37 recite

an image processing apparatus and method, respectively, in which the supply of clock signal to a pixel processing circuit is stopped when it is judged that the circuit will not perform a rewrite of depth data stored in a storage circuit for a corresponding pixel.

As explained above, Huxley does not teach or suggest a system in which a clock signal is stopped to stop the operation of a pixel processing circuit after determining that it will not perform a rewrite of depth data in a storage circuit. Similarly, the combined teachings of Dawson et al. and Kiyoto lack any teaching or suggestion of an image processing system in which clock signals for individual pixel processing circuits in a block of such circuits to be processed simultaneously are selectively stopped based on a judgment that a certain operation (i.e., depth data rewrite) is not required of such pixel processing circuit.

Independent claims 21 and 40 are allowable for at least the same reasons explained above in connection with the Examiner's rejections of independent claims 6, 17, 27 and 36, which separately recite similar features of the Applicant's invention.

Accordingly, reconsideration and withdrawal of the rejection of claims 11 to 13, 15 to 19, 21, 31 to 33, 35 to 38 and 40 based on Dawson, Huxley and Kiyoto are respectfully requested.

Claims 14, 20, 34 and 39 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dawson et al. in view of Huxley and Kiyoto, and further in view of Duluk, Jr. The Examiner relies upon Duluk, Jr. for a teaching of a flag storage portion connected to the shift register in series. This rejection is respectfully traversed for the following reasons.

Claims 14, 20, 34 and 39 are dependent, directly or indirectly, on independent claims 11, 17, 31 and 36, respectively. Therefore, it is respectfully submitted that these claims are allowable over the cited references for at least the same reasons explained above concerning these independent claims. It is further noted that the image processing system disclosed by Duluk, Jr. fails to remedy the various deficiencies in the combined teachings of Dawson et al., Huxley and Kiyoto, as explained above.

Applicant respectfully submits that all of the pending claims 1 to 40 are now in condition for allowance, and requests that a timely Notice of Allowance be issued for this application.

If the Examiner has any comments or suggestions that could place this application into even better form, the Examiner is encouraged to contact the Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted by:

Dated: **October 17, 2001**

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title of the application has been amended to read as follows:

--IMAGE PROCESSING APPARATUS AND METHOD OF [THE SAME] PROCESSING IMAGES THAT STOPS OPERATION OF PIXEL PROCESSING CIRCUITS WHEN PIXEL DATA TO BE PROCESSED IS NOT NEEDED--.

IN THE SPECIFICATION:

The paragraph beginning at line 24 of page 1 has been amended as follows:

-- One of the rendering methods is polygon rendering. In this method, a three-dimensional model is expressed as a [an] composite of triangular unit graphics (polygons). By drawing the polygons as units, the colors of the pixels of the display screen are decided. --

The paragraph beginning at line 17 of page 26 has been amended as follows:

-- The operation sub-blocks 203_1 to 203_8 perform the above blending and output the (R, G, B, α) data $S203_1$ to $S203_8$ [203_8] only when results of the level detection of the val data $S220_1$ to $S220_8$ by the clock enablers 213_1 to 213_8 are "1." --

The paragraph beginning at line 23 of page 26 has been amended as follows:

-- The operation block 204 has the operation sub-blocks 204_1 to 204_8 and performs a z-comparison for the input (R, G, B, α) data $S203_1$ to $S203_8$ by using the content of the z-data stored in the z-buffer 22. When the image drawn by the (R, G, B, α) data $S203_1$ to $S203_8$ is positioned closer to the viewing point than the image drawn in the display buffer 21 the previous time, the operation block 204 updates the z-buffer 22 and outputs the (R, G, B, α) data $S203_1$ to $S203_8$ as the (R, G, B, α) data $S204_1$ to $\underline{S204_8}$ [204_8] to the operation sub-blocks 205_1 to 205_8 of the operation block 205. --

The paragraph beginning at line 15 of page 27 has been amended as follows:

-- The operation block 205 has the operation sub-blocks 205_1 to 205_8, blends the (R, G, B, α) of the data $S204_1$ to $S204_8$ and the (R, G, B) data already stored in the display buffer 21 by the blending ratio indicated in the α data included in the (R, G, B, α) data $S204_1$ to $S204_8$, and writes the blended (R, G, B) data $S205_1$ to $\underline{S205_8}$ [205_8] in the display buffer. --

The paragraph beginning at line 25 of page 29 has been amended as follows:

-- Here, a case of, for example, simultaneous processing on 8 pixels in a block 31 shown in Fig. 12 [Fig. 6] will be considered. In this case, the val data $S220_1$, $S220_2$, $S220_3$, $S220_5$, and $S220_6$ indicate "0" and the val data $S220_4$, $S220_7$, and $S220_8$ indicate

"1." --

The paragraph beginning at line 8 of page 30 has been amended as follows:

-- Then in the clock enablers 210_1 to 210_8, the levels of the respective val data $S220_1$ to $\underline{S220_8}$ [220_8] are detected. Specifically, "1" is detected in the clock enablers 210_4, 210_7, and 210_8 and "0" is detected in the clock enablers 210_1, 210_2, 210_3, 210_5, and 210_6. --

The paragraph beginning at line 25 of page 30 has been amended as follows:

-- Next, the clock enablers $\underline{211_1 \text{ to } 211_8}$ [210_1 to 210_8] of the operation sub-blocks 201_1 to 201_8 detect the levels of the respective val data $S220_1$ to $S220_8$. --

The paragraph beginning at line 10 of page 31 has been amended as follows:

-- On the other hand, no operation is performed [is] in the operation sub-blocks 201_1, 201_2, 201_3, 201_5, and 201_6. --

The paragraph beginning at line 8 of page 32 has been amended as follows:

-- Next, the clock enablers $\underline{213_1 \text{ to } 213_8}$ [212_1 to 212_8] of the operation sub-blocks 203_1 to 203_8 detect the levels of the respective val data $S220_1$ to $S220_8$. --

The paragraph beginning at line 11 of page 32 has been amended as follows:

-- Then, based on the detection results, only the operation sub-blocks 203_4, 203_7, and 203_8 blend the texture data (R, G, B, α) $S202_4$, $\underline{S202_7}$ [202_7], and $\underline{S202_8}$[202_8] input from the operation block 202 and the (R, G, B) data included in the DDA data S11 from the triangle DDA circuit 11 by the blending ratio indicated by the α data (texture α) included in the (R, G, B, α) data $S202_4$, $\underline{S202_7}$ [202_7], and $\underline{S202_8}$[202_8] to generate the blended data (R, G, B). --

The paragraph beginning at line 14 of page 36 has been amended as follows:

-- Here, the DDA set-up circuit 10, the texture engine circuit 12, the CRT controller circuit 14, the RAMDAC circuit 15, the DRAM 16, and the SRAM 17 are the same <u>as</u> [in] those explained in the first embodiment. --

The paragraph beginning at line 6 of page 44 has been amended as follows:

-- The operation block 500 has operation sub-blocks 501_1 to 500_8 and receives as input the DDA data S11 from the triangle DDA circuit <u>11</u> shown in Fig. 7. --

The paragraph beginning at line 9 of page 44 has been amended as follows:

-- The operation sub-blocks 501_1 to 500_8 detect the levels of the val data $S220_1$ to $S220_8$ included in the DDA data S11 in the respective clock enablers $\underline{510_1 \text{ to } 510_8}$ [214_1 to

214_8] and perform the z-comparison when the level is "1" (when the pixel is inside a triangle being processed), while do not perform the z-comparison when the level is not "1." --

The paragraph beginning at line 6 of page 47 has been amended as follows:

-- The operation block 503 has operation sub-blocks 503_1 to 503_8, outputs a read request including the texture coordinate data (u, v) generated in the operation block 502 to the SRAM 17 or DRAM 16 via the memory I/F circuit 13, and reads the texture data stored in the SRAM 17 or the texture buffer 20 via the memory I/F circuit 513 [13] to obtain the (R, G, B, α) data S17 stored in the texture address corresponding to the (u, v) data. --

The paragraph beginning at line 7 of page 49 has been amended as follows:

-- First, the clock enablers 510_1 to 510_8 [214_1 to 214_8] of the operation sub-blocks 500_1 to 500_8 detect the levels of the val data $S220_1$ to $S220_8$ included in the DDA data S11. When the detected level is "1" (when the pixel is inside the triangle being processed), the z-comparison is performed. --

The paragraph beginning at line 2 of page 52 has been amended as follows:

-- Next, in the clock enablers 515_1 to 515_8 [215_1 to 215_8] of the operation sub-

blocks 505_1 to 505_8, the levels of the val data $S220_1$ to $S220_8$ and $S500a_1$ to $S500a_8$ are detected. Only when both of the levels are "1," the (R, G, B, α) data $S504_1$ to $S504_8$ and the (R, G, B) data already stored in the display buffer 21 are blended by the blending ratio indicated by the α data included in the respective (R, G, B, α) data $S504_1$ to $S504_8$. The blended (R, G, B) data $S505_1$ to $S505_8$ are written in the display buffer 21. --

The paragraph beginning at line 5 of page 53 has been amended as follows:

-- For example, in the above second embodiment, as shown in Fig. 6, an example was given of the case where 8 pixels of data were simultaneously processed in the operation blocks of the texture engine circuit 12 and the memory I/F circuit 413[,]. However, as shown in Fig. 9 [however], 1 pixel of data may be processed in the operation blocks as well. --

The paragraph beginning at line 18 of page 53 has been amended as follows:

-- Also, in the above third embodiment, as shown in Fig. 8, an example was given of the case where 8 pixels of data were simultaneously processed in the operation blocks of the texture engine circuit 512 and the memory I/F circuit 513 [, however]. However, as shown in Fig. 10, 1 pixel of data may also be processed in the operation blocks. --

The paragraph beginning at line 4 of page 55 has been amended as follows:

-- Also, in the above embodiments, as shown in Fig. 2, an example was given of using the DDA data S11 in which the val data was added as valid instruction data to the data (z, R, G, B, α, s, t, q) to be image processed [, however]. However, the (z, R, G, B, α, s, t, q) data and the val data may be handled as separate independent data. --

IN THE CLAIMS:

Claims 1 to 7, 9 to 12, 14, 16, 18, 21 to 23, 25, 27, 28, 31, 32, 35, 37, 39 and 40 have been amended as follows:

1. (Amended) An image processing apparatus comprising:

a plurality of pixel processing circuits, each provided for processing each of a plurality of pixel data to be processed simultaneously, for processing a plurality of input pixel data in parallel; and

a control circuit for stopping the operation of at least one of said pixel processing circuits [circuit] when the processing of said pixel data to be processed in the pixel processing circuit is not needed.

2. (Amended) An image processing apparatus as set forth in claim 1, wherein:

said pixel processing circuits operate [circuit operates] on the basis of a clock signal[,]; and

said control circuit supplies said pixel processing circuits [circuit] with said clock

signal when judging the pixel processing is needed and stops the supply of said clock signal to said at least one of said pixel processing circuits [circuit] when judging the pixel processing is not needed.

3. (Amended) An image processing apparatus as set forth in claim 2, wherein each of said pixel processing circuits comprises a plurality of [series connected] processing circuits connected in series to form [formed as] a pipeline circuit.

4. (Amended) An image processing apparatus as set forth in claim 3, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control [said] pipeline processing within the pixel processing circuit and the supply of said clock signal.

5. (Amended) An image processing apparatus as set forth in claim 1, wherein each of said pixel processing circuits [circuit] performs processing with respect to pixel data of red (R), green (G), and blue (B) of a pixel.

6. (Amended) An image processing apparatus for expressing an image to be

displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each [the same said] graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a pixel position judging circuit for judging whether or not a corresponding pixel is positioned within said graphic unit for each of the plurality of pixel data to be processed simultaneously;

a plurality of pixel processing circuits for processing a plurality of pixel data to be processed simultaneously mutually in parallel; and

a control circuit for stopping the operation of the pixel processing circuits other than processing circuits for processing pixel data of pixels positioned within the graphic unit to be processed among said plurality of pixel processing circuits on the basis of the results of the judgement of said pixel position judging circuit.

7. (Amended) An image processing apparatus as set forth in claim 6, wherein:

each of said pixel processing circuits [circuit] operates on the basis of a clock signal; and

said control circuit supplies said clock signal to pixel processing circuits

processing the pixel data of pixels positioned inside the graphic unit to be processed, and stops the supply of said clock signal to pixel processing circuits processing the pixel data of pixels not positioned inside the graphic unit to be processed.

9. (Amended) An image processing apparatus as set forth in claim 8, wherein each of said plurality of processing circuits connected in series within each said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

10. (Amended) An image processing apparatus as set forth in claim 6, wherein:

said pixel position judging circuit adds validity data indicating the result of the judgement to pixel data processed by said pixel processing circuits; and

said control circuit judges based on the validity data whether to stop the operation of said pixel processing circuits.

11. (Amended) An image processing apparatus comprising:

a plurality of pixel [image] processing circuits, provided for a plurality of pixels to be processed simultaneously, for blending a plurality of first pixel data and a corresponding plurality of second pixel data by blending ratios indicated by a blending

ratio data set for each pixel to produce a plurality of third pixel data; and

a control circuit for judging whether or not said pixel processing circuits will perform said blending and stopping the operation of said pixel processing circuits when judging that said blending will not be performed.

12. (Amended) An image processing apparatus as set forth in claim 11, wherein:

each of said pixel processing circuits operates on the basis of a clock signal; and

said control circuit supplies each respective [said] pixel processing circuit with said clock signal when judging that said pixel processing circuit [it] will perform blending and stops the supply of said clock signal to said pixel processing circuit when judging that it will not perform said blending.

14. (Amended) An image processing apparatus as set forth in claim 13, wherein each of said plurality of processing circuits connected in series within each said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

16. (Amended) An image processing apparatus for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape,

processing pixel data of a plurality of pixels positioned within each [the same said] graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a plurality of image processing circuits, provided for a plurality of pixels to be processed simultaneously, for blending a plurality of first pixel data and a corresponding plurality of second pixel data by a blending ratio indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data; and

a control circuit for judging whether or not a corresponding pixel is positioned within said [a] graphic unit to be processed for each of said plurality of pixels to be processed simultaneously and stopping the operation of a pixel processing circuit when judging that said corresponding pixel is not positioned within said graphic unit or when judging that said blending will not be [not] performed on the basis of said blending ratio data.

18. (Amended) An image processing apparatus as set forth in claim 17, wherein:

said pixel processing circuit operates on the basis of a clock signal; and

said control circuit supplies said pixel processing circuit with said clock signal when judging to rewrite the third pixel data stored in the storage circuit with the second

pixel data and stopping the supply of said clock signal to the pixel processing circuit when judging not to rewrite the third pixel data stored in the storage circuit by the second pixel data.

21. (Amended) An image processing apparatus for expressing an image to be displayed [display] on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each [the same] graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a storage circuit;

a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, for producing a plurality of second pixel data from a plurality of first pixel data;

a comparing circuit for comparing a plurality of [said] first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in said storage circuit in correspondence with said plurality of first depth data;

a control circuit for judging whether or not a corresponding pixel is positioned

within said graphic unit to be processed for each of said plurality of pixels to be processed simultaneously, judging whether or not to rewrite said third pixel data corresponding to said second depth data stored in said storage circuit with said second pixel data on the basis of the result of the comparison, and stopping the operation of at least one of said [a] pixel processing circuits [circuit] when judging that the [said] corresponding pixel is not positioned within said graphic unit or when judging not to rewrite.

22. (Amended) An image processing method for performing image processing by using pixel processing circuits, each provided for each of a plurality of pixels to be processed simultaneously, for processing a plurality of input pixel data in parallel, comprising the steps of:

judging whether or not on the basis of said pixel data the pixel processing of said processing circuits is needed[,]; and

stopping operation of at least one of said pixel processing circuits [circuit] when judging the pixel processing of said at least one processing circuit is not needed.

23. (Amended) An image processing method as set forth in claim 22, further comprising the steps of:

supplying said pixel processing circuit with a clock signal when judging the pixel

processing is needed; and

stopping the supply of said clock signal to said pixel processing circuit when judging the pixel processing is not needed.

25. (Amended) An image processing method as set forth in claim 24, wherein each of said plurality of processing circuits connected in series within each of said pixel processing circuits [circuit] has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

27. (Amended) An image processing method for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each [the same said] graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of the plurality of pixel data to be processed simultaneously;

processing a plurality of pixel data to be processed simultaneously mutually in parallel in a plurality of pixel processing circuits; and

stopping the operation of the pixel processing circuits other than processing circuits for processing pixel data of pixels positioned within the graphic unit to be processed among said plurality of pixel processing circuits on the basis of the results of the judgement.

28. (Amended) An image processing method as set forth in claim 27, further comprising the steps of:

supplying a clock signal to the pixel processing circuits processing the pixel data of pixels positioned inside the graphic unit to be processed[,]; and

stopping the supply of said clock signal to pixel processing circuits processing the pixel data of pixels not positioned inside the graphic unit to be processed.

29. (Unchanged) An image processing method as set forth in claim 28, wherein each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

31. (Amended) An image processing method comprising the steps of:

using a plurality of pixel processing circuits provided for a plurality of pixels to be

processed simultaneously to blend a plurality of first pixel data and a plurality of second pixel data by blending ratios indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data[,];

judging based on said blending ratio data whether to perform said blending by said pixel processing circuits[,]; and

stopping the operation of at least one of said [the corresponding] pixel processing circuits when judging that said at least one pixel processing circuit [they] will not perform said blending.

32. (Amended) An image processing method as set forth in claim 31, further comprising the steps of:

[operating,]

supplying a corresponding pixel processing circuit with a clock signal when judging that said corresponding pixel processing circuit [it] will perform blending[,]; and

stopping the supply of said clock signal to at least one of said [a corresponding] pixel processing circuits [circuit] when judging that said at least one pixel processing circuit [it] will not perform said blending.

35. (Amended) An image processing method for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape,

processing pixel data of a plurality of pixels positioned within each [the same said] graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

using a plurality of image processing circuits, provided for a plurality of pixels to be processed simultaneously, to blend a plurality of first pixel data and a plurality of second pixel data by a blending ratio indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data[,];

judging whether or not a corresponding pixel is positioned within a corresponding one of said graphic units [unit] for each of said plurality of pixels to be processed simultaneously; and

stopping the operation of at least one of said [a] pixel processing circuits [circuit] when judging that the [said] corresponding pixel is not positioned within said graphic unit to be processed or when judging that said blending will not be [not] performed on the basis of said blending ratio data.

37. (Amended) An image processing method as set forth in claim 36, further comprising the steps of:

supplying said pixel processing circuit with a clock signal when judging to rewrite

the third pixel data stored in the storage circuit with the second pixel data[,]; and

stopping the supply of said clock signal to the pixel processing circuit when judging not to rewrite the third pixel data stored in the storage circuit by the second pixel data.

39. (Amended) An image processing method as set forth in claim 38 [37], wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

40. (Amended) An image processing method for expressing an image to be displayed [display] on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each [the same] graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

using a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, to produce a plurality of second pixel data from a plurality

of first pixel data;

comparing a plurality of said first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in a storage circuit in correspondence with said plurality of first depth data; [and]

judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of said plurality of pixels to be processed simultaneously, judging whether or not to rewrite said third pixel data corresponding to said second depth data stored in said storage circuit with said second pixel data on the basis of the result of the comparison[,]; and

stopping the operation of at least one of said [a] pixel processing circuits [circuit] when judging that the [said] corresponding pixel is not positioned within said graphic unit to be processed or when judging not to rewrite.

FIG. 1

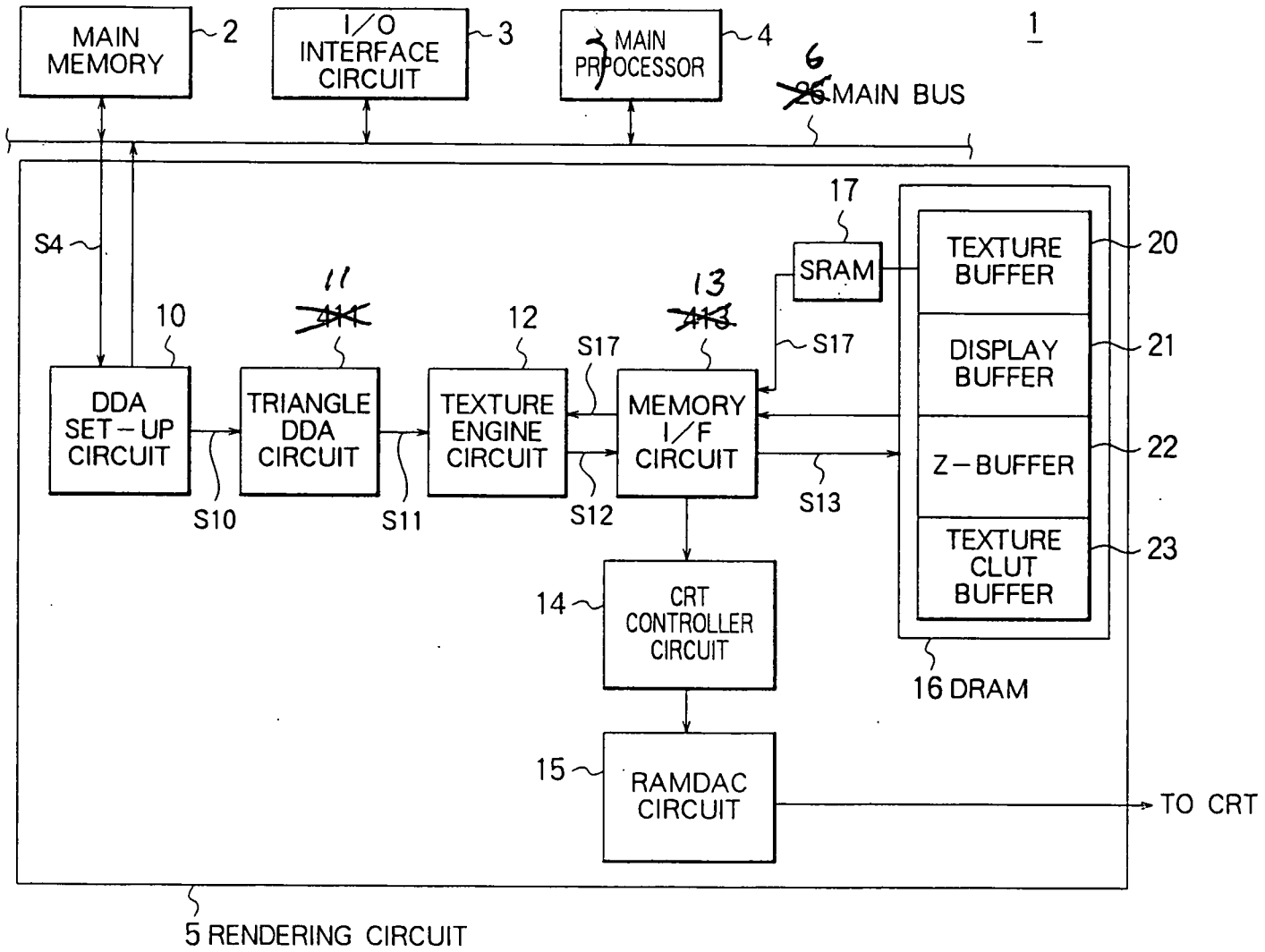

MAIN MEMORY
2
I/O INTERFACE CIRCUIT
3
MAIN PROCESSOR
4
1
6
MAIN BUS
S4
17
SRAM
TEXTURE BUFFER
20
DISPLAY BUFFER
21
Z-BUFFER
22
TEXTURE CLUT BUFFER
23
16 DRAM
10
DDA SET-UP CIRCUIT
11
TRIANGLE DDA CIRCUIT
12
TEXTURE ENGINE CIRCUIT
13
MEMORY I/F CIRCUIT
S10
S11
S12
S13
S17
S17
14
CRT CONTROLLER CIRCUIT
15
RAMDAC CIRCUIT
TO CRT
5 RENDERING CIRCUIT

FIG. 4

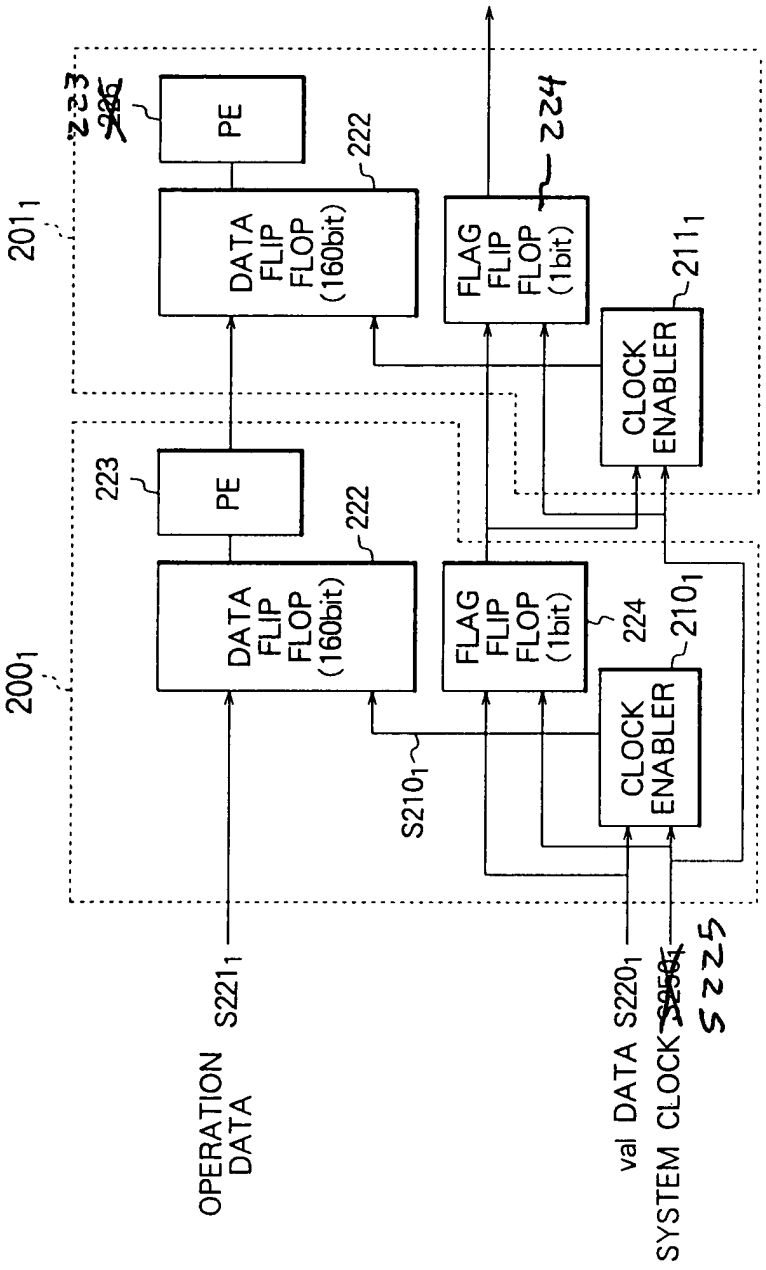

200_1
201_1
223
PE
222
DATA FLIP FLOP (160bit)
224
FLAG FLIP FLOP (1bit)
210_1
211_1
CLOCK ENABLER
$S210_1$
OPERATION DATA
$S221_1$
val DATA $S220_1$
SYSTEM CLOCK
S225

FIG. 5

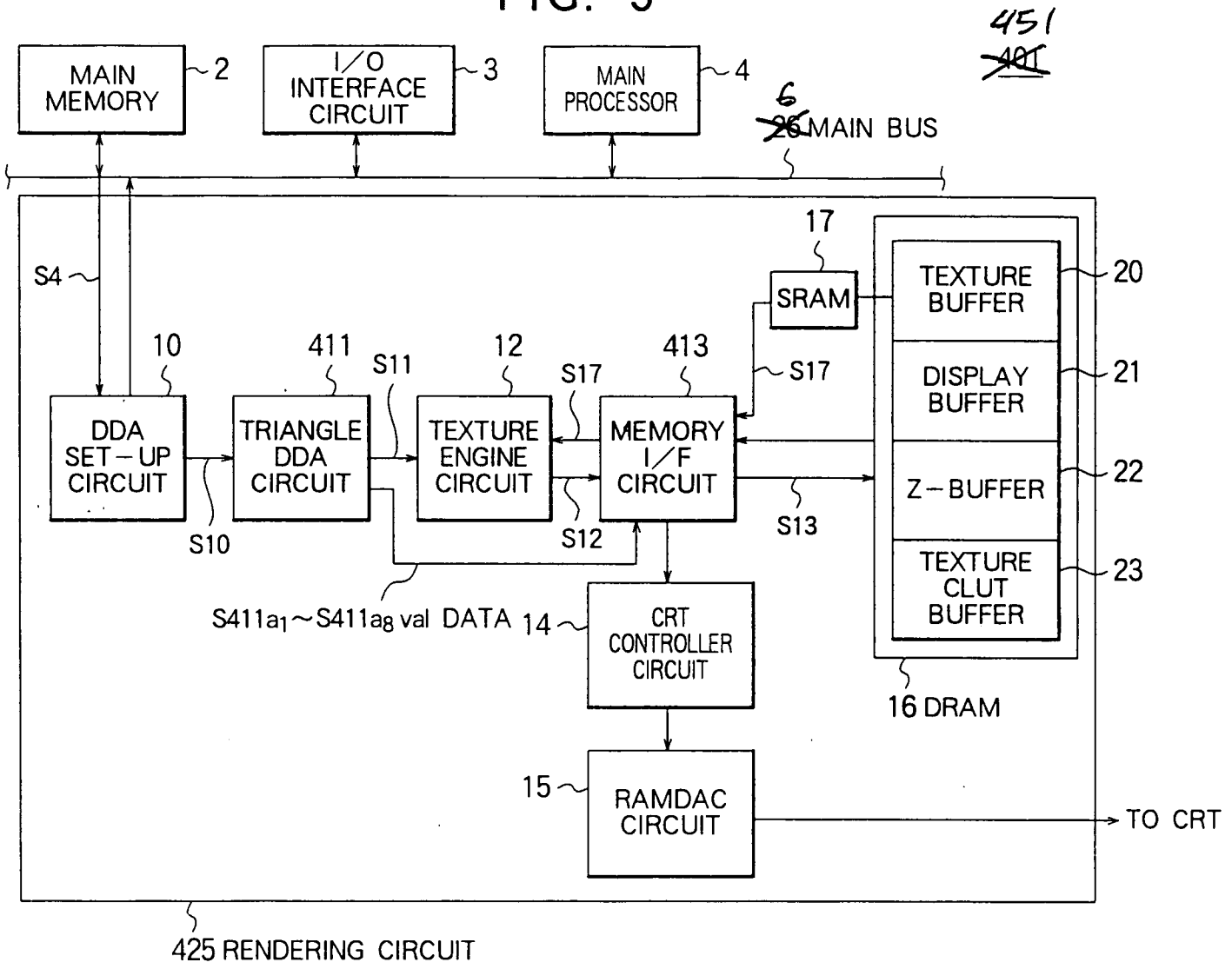

451
MAIN MEMORY
2
I/O INTERFACE CIRCUIT
3
MAIN PROCESSOR
4
6
MAIN BUS
17
SRAM
TEXTURE BUFFER
20
DISPLAY BUFFER
21
Z-BUFFER
22
TEXTURE CLUT BUFFER
23
16 DRAM
S4
10
DDA SET-UP CIRCUIT
S10
411
TRIANGLE DDA CIRCUIT
S11
12
TEXTURE ENGINE CIRCUIT
S17
413
MEMORY I/F CIRCUIT
S17
S12
S13
S411a1~S411a8 val DATA
14
CRT CONTROLLER CIRCUIT
15
RAMDAC CIRCUIT
TO CRT
425 RENDERING CIRCUIT

FIG. 7

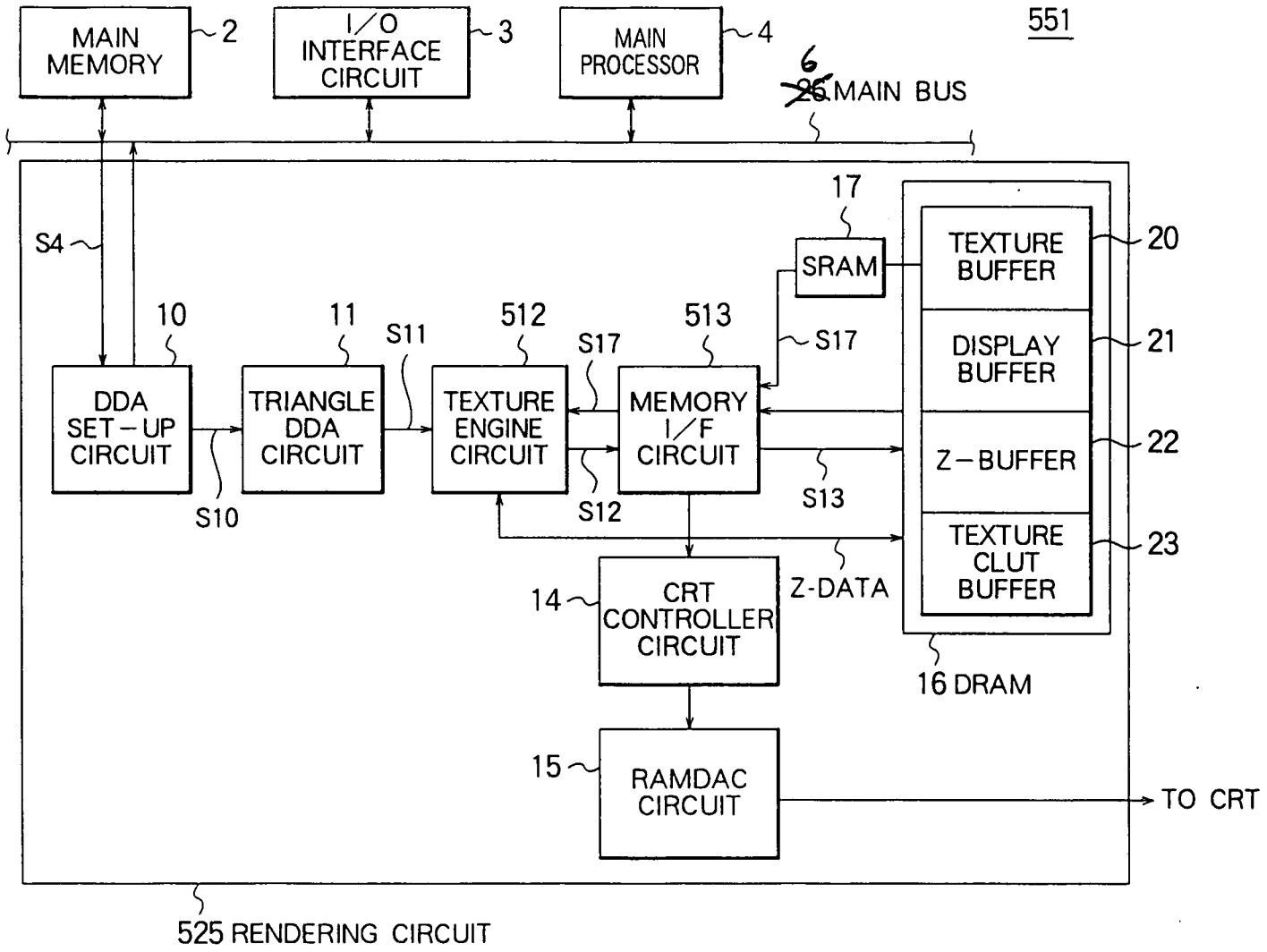

MAIN MEMORY
2
I/O INTERFACE CIRCUIT
3
MAIN PROCESSOR
4
551
6
MAIN BUS
S4
17
SRAM
TEXTURE BUFFER
20
DISPLAY BUFFER
21
Z-BUFFER
22
TEXTURE CLUT BUFFER
23
10
11
S11
512
S17
513
S17
DDA SET-UP CIRCUIT
TRIANGLE DDA CIRCUIT
TEXTURE ENGINE CIRCUIT
MEMORY I/F CIRCUIT
S10
S12
S13
Z-DATA
14
CRT CONTROLLER CIRCUIT
16 DRAM
15
RAMDAC CIRCUIT
TO CRT
525 RENDERING CIRCUIT

FIG. 8

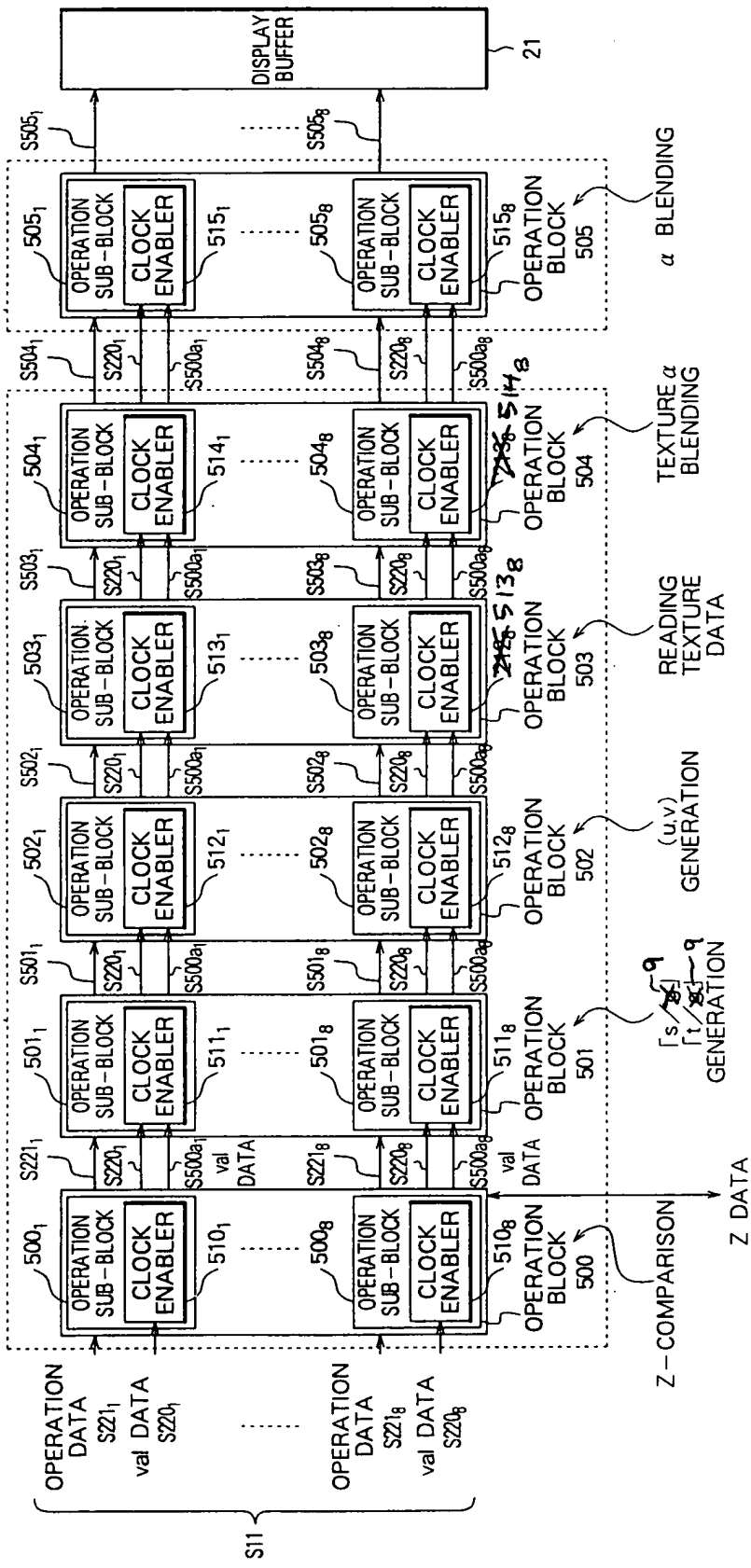
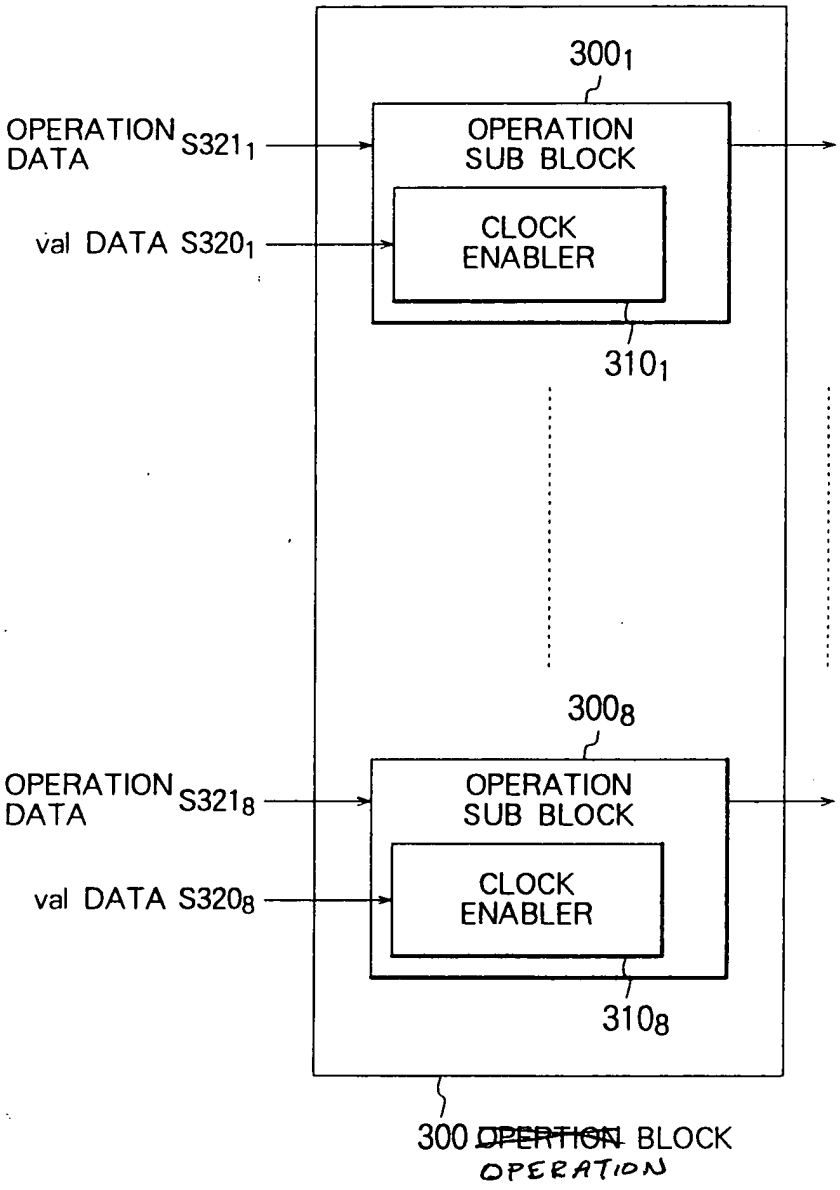

512 TEXTURE ENGINE CIRCUIT
513 MEMORY I/F CIRCUIT
DISPLAY BUFFER
21
OPERATION BLOCK
OPERATION SUB-BLOCK
CLOCK ENABLER
500
501
502
503
504
505
α BLENDING
TEXTURE α BLENDING
READING TEXTURE DATA
(u,v) GENERATION
[s/t] GENERATION
Z-COMPARISON
Z DATA
val DATA
OPERATION DATA
S11

FIG. 11


300_1
OPERATION DATA $S321_1$
OPERATION SUB BLOCK
CLOCK ENABLER
val DATA $S320_1$
310_1
300_8
OPERATION DATA $S321_8$
OPERATION SUB BLOCK
CLOCK ENABLER
val DATA $S320_8$
310_8
300 ~~OPERTION~~ BLOCK
OPERATION